(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 684 650 B1

(12) EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention of the grant of the patent:
29.08.2001 Bulletin 2001/35

(21) Application number: **95107868.2**

(22) Date of filing: **23.05.1995**

(51) Int Cl.[7]: **H01L 29/786**, H01L 21/336, H01L 29/78, H01L 29/49, H01L 29/51, H01L 23/532, H01L 21/321, H01L 21/768

(54) SiGe thin film semiconductor device with SiGe layer structure and method of fabrication

SiGe-Dünnfilm-Halbleiteranordnung mit SiGe Schichtstruktur und Verfahren zur Herstellung

Dispositif semi-conducteur à couche mince avec structure d'une couche de SiGe et sa méthode de fabrication

(84) Designated Contracting States:
DE FR NL

(30) Priority: **24.05.1994 JP 10923394**

(43) Date of publication of application:
29.11.1995 Bulletin 1995/48

(60) Divisional application:
99107808.0 / 0 935 292

(73) Proprietor: **MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.**
Kadoma-shi, Osaka 571-8501 (JP)

(72) Inventor: **Tsutsu, Hiroshi**
Osaka-shi, Osaka (JP)

(74) Representative: **Kügele, Bernhard et al**
NOVAPAT-CABINET CHEREAU,
9, Rue du Valais
1202 Genève (CH)

(56) References cited:
EP-A- 0 061 388
EP-A- 0 449 620
EP-A- 0 587 520

- **JOURNAL OF APPLIED PHYSICS, 1 FEB. 1994, USA, vol. 75, no. 3, ISSN 0021-8979, pages 1764-1770, XP000615103 PARK S -G ET AL: "Kinetics and mechanism of wet oxidation of Ge/sub x/Si/sub 1-x/ alloys"**
- **JAPANESE JOURNAL OF APPLIED PHYSICS, PART 2 (LETTERS), SEPT. 1986, JAPAN, vol. 25, no. 9, ISSN 0021-4922, pages L718-L721, XP000021844 OKADA H ET AL: "High-mobility amorphous-silicon MOS transistors"**
- **PATENT ABSTRACTS OF JAPAN vol. 013, no. 564 (E-860), 14 December 1989 & JP 01 235276 A (SONY CORP), 20 September 1989,**
- **IEEE ELECTRON DEVICE LETTERS, vol. 12, no. 11, 1 November 1991, pages 584-586, XP000228169 TSU-JAE KING ET AL: "PMOS TRANSISTORS IN LPCVD POLYCRYSTALLINE SILICON-GERMANIUM FILMS"**
- **OPTICAL ENGINEERING, AUG. 1993, USA, vol. 32, no. 8, ISSN 0091-3286, pages 1798-1802, XP000615105 HUANG-CHUNG CHENG ET AL: "Characteristics of polycrystalline silicon thin-film transistors with thin oxide/nitride gate structures"**

EP 0 684 650 B1

Printed by Jouve, 75001 PARIS (FR)

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention:

[0001] The present invention relates to a thin film semiconductor device, and a method for fabricating such a thin film semiconductor device. In particular, the present invention relates to a thin film semiconductor device used for a liquid crystal display device (hereinafter, abbreviated as "LCD") for driving liquid crystal, a sensor for reading images, a load of RAM (Random Access Memory) and the like, and a method for fabricating such a thin film semiconductor device.

2. Description of the Related Art:

[0002] A thin film semiconductor device includes a thin film semiconductor layer formed on a substrate having an insulating surface such as a quartz substrate or a glass substrate. A thin film transistor (TFT) is utilized in various fields. Hereinafter, a conventional example of a polycrystalline silicon thin film transistor, which has been developed for the use for a liquid crystal display (LCD), will be described.

[0003] Recently, in the field of the liquid crystal display using the thin film transistor, a polycrystalline silicon thin film transistor (hereinafter, referred to as a "low-temperature poly-Si TFT"), which can be fabricated at a relatively low temperature (about 600°C or less) at which inexpensive glass substrates can be used instead of expensive quartz substrates, has attracted attention. However, one of the important problems to be solved of the low-temperature poly-Si TFT is the improvement in quality of a gate insulating film. Therefore, various gate insulating films have been examined.

[0004] A low-temperature poly-Si TFT described in "Society of Information Display International symposium Digest of Technical Papers / Volume XXIV (1993) pp. 387 - 390" will be briefly described as a conventional example, with reference to Figures **4A** to **4D**.

[0005] The low-temperature poly Si TFT is fabricated as follows.

[0006] First, an amorphous silicon film is deposited on a top surface of a substrate **12**, and then it is irradiated with a laser light so as to locally heat and melt the amorphous silicon film. As a result, the amorphous silicon film is crystallized, thereby obtaining a polycrystalline silicon film **13**. Thereafter, the polycrystalline silicon film **13** is patterned into an island shape by photolithography and etching (Figure **4A**).

[0007] Next, after a gate insulating film **14** which consists of an SiO_2 layer is formed on the polycrystalline silicon film **13** by using an ECR-CVD method (Figure **4B**), a gate electrode **15** made of tantalum (Ta) is formed on the gate insulating film **14**. Thereafter, by using the gate electrode **15** as a mask, impurities serving as donors or acceptors are introduced into the polycrystalline silicon film **13** by ion doping in which mass separation is not conducted, thereby forming a source region **16** and a drain region **17** (Figure **4C**). After forming an interlevel insulating film **18**, a source electrode **19** and a drain electrode **20** are formed on the insulating film **18**. As a result, a low-temperature poly-Si TFT shown in Figure **4D** is fabricated.

[0008] In the conventional low-temperature poly-Si TFT shown in Figures **4A** to **4D**, the gate insulating film **14** which consists of an SiO_2 film is deposited by the ECR-CVD (Electron Cyclotron Resonance Chemical Vapor Deposition) method. Therefore, it has been reported that the low-temperature poly-Si TFT has good characteristics as compared with SiO_2 deposited by an AP-CVD (Atmospheric Pressure Chemical Vapor Deposition) method or LTO (low temperature oxide). However, even if the ECR-CVD method is used, the most important interface of semiconductor/insulating film, which affects device characteristics, becomes remarkably unstable. The reason for this is that the SiO_2 layer functioning as the gate insulating film **14** is deposited after the polycrystalline silicon layer **13** is formed and the substrate is subjected to processes such as a cleaning process. The state of the interface between the insulating film deposited by a CVD method and the semiconductor may greatly change due to various conditions such as a cleaning condition before depositing the insulating film, waiting time after the cleaning until deposition, an atmosphere immediately before the deposition. As a result, the interfacial states at the semiconductor/insulating film interface may be remarkably degraded. Thus, characteristics of a thin film transistor are prone to be degraded. Moreover, in order to perfectly control the interfacial states density, it is necessary to strictly control the fabrication conditions. Therefore, this method is not suitable for mass production. Furthermore, the method has another problem that the production yield is low due to pin holes of the insulating film and the like since the gate insulating film is obtained by a CVD method.

[0009] In the field of LSI, a thermal oxide film made of silicon is generally utilized as a gate insulating film in order that the interfacial states density is controlled at a predetermined level or a lower level. However, growth of such a thermal oxide film requires high temperature process. Therefore, it is necessary to use an expensive quartz substrate which induces no strain even in a high-temperature process, resulting in an increase in the fabrication cost.

[0010] The document Patent Abtracts of Japan, vol. 13, no.564 & JP 01 235 276 further describes a thin film semiconductor device (TFT) according to the preamble of present claim 1 and having a silicon substrate with a protective SiO2 film. The formation of a gate insulating film is described by oxidising the silicon thin film into which germanium is implanted. However, the Ge-concentration in the silicon thin film is 0.5 - 2.0 atom%. EP-

A-0 587 520 shows also a device according to the preamble of claim 1. The gate oxide does, however, not comprise Ge.

SUMMARY OF THE INVENTION

[0011] The present invention thus concerns a thin film semiconductor device as defined in claim 1, and also a corresponding method of fabricating as defined in claim 4.

[0012] Thus, the invention described herein makes possible the advantages of (1) providing a thin film transistor having excellent performance and high reliability, which can use a low-cost glass substrate as a substrate and has a clean interface of semiconductor/insulating film, (2) providing a method for fabricating such a thin film transistor, and (3) a semiconductor device.

[0013] These and other advantages of the present invention will become apparent to those skilled in the art upon reading and understanding the following detailed description with reference to the accompanying figures.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] Figures **1A** to **1D** are schematic cross-sectional views each showing a main step of a fabrication method of a thin film transistor according to the present invention.

[0015] Figure **2A** is a schematic cross-sectional view showing another thin film transistor according to the present invention.

[0016] Figure **2B** is a schematic cross-sectional view showing still another thin film transistor according to the present invention.

[0017] Figures **3A** to **3D** are schematic cross-sectional view showing still another thin film transistor according to the present invention.

[0018] Figures **4A** to **4D** are schematic cross-sectional views each showing a main step of a fabrication method of a conventional thin film transistor.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0019] Hereinafter, the present invention will be described by way of illustrative examples with reference to the drawings.

Example 1

[0020] With reference to Figures **1A** to **1D**, a first example of a thin film semiconductor device according to the present invention will be described. In this example, a glass substrate (glass #1737, fabricated by Corning Inc.) **1**, on which an SiO_2 film acting as a buffer layer (not shown) is deposited in order to prevent the diffusion of impurities from the glass substrate, is used. The glass substrate **1** has a strain point of 667°C. From the viewpoint of reduction in cost, it is preferable to use an inexpensive glass having a strain point as low as possible as the glass substrate **1**. Considering expansion or warp of the glass substrate **1** due to heat, it is preferable that the strain point of the glass substrate **1** is about +50°C or more of the process maximum temperature.

[0021] First, an amorphous silicon-germanium film containing germanium at a concentration of 25% (hereinafter, referred to as an "a-$Si_{0.75}Ge_{0.25}$" film) is grown on the glass substrate **1** to a thickness of 100 nm. The a-$Si_{0.75}Ge_{0.25}$ film is formed by a CVD method using, for example, disilane (Si_2H_6) and germane (GeH_4) as material gases. Typically, the flow rate of disilane is in the range of 20 to 50 sccm, and the flow rate of germane is 10 to 30 sccm. It goes without saying that the flow rate of the gas changes depending on the size of the chamber and the like. It is preferable that the temperature of the glass substrate **1** during growth of the film is set to be in the range of 450°C to 600°C.

[0022] Next, the a-$Si_{0.75}Ge_{0.25}$ film is patterned to form an island region having the size in accordance with the size of a transistor to be formed. The size of one island region is, for example, 10 μm x 50 μm. In Figure **1A**, only one island region is shown. In actual, however, a plurality of island regions can be simultaneously formed. The patterning of the a-$Si_{0.75}Ge_{0.25}$ film can be carried out using normal photolithography and etching. As an etchant, for example, a mixture of hydrofluoric acid and nitric acid and the like can be used. In the case where dry etching is conducted, CF_4 or SF_6 to which O_2 is added is used.

[0023] Thereafter, an excimer laser light having a wavelength of 308 nm is radiated onto the a-$Si_{0.75}Ge_{0.25}$ film so as to melt/solidify (crystallize) the a-$Si_{0.75}Ge_{0.25}$ film. In this way, a semiconductor layer 2 made of polycrystalline silicon-germanium (hereinafter, referred to as "poly-$Si_{0.75}Ge_{0.25}$") is obtained. While the a-$Si_{0.75}Ge_{0.25}$ film is crystallized after being patterned in Example 1, the a-$Si_{0.75}Ge_{0.25}$ film may be crystallized before being pattemed.

[0024] Next, the glass substrate **1** is inserted into a furnace at 600°C. Pure water held at 95°C is subjected to bubbling with nitrogen or gaseous oxygen. By using steam obtained by the bubbling, the surface of the semiconductor layer **2** is thermally oxidized for two hours in the furnace. By the thermal oxidation, as shown in Figure **1B**, a thermal oxide film having a thickness of about 100 nm is formed. The thus obtained thermal oxide film, which is made of $Si_{0.75}Ge_{0.25}O_2$, is used as a gate insulating film **3**. The thickness of the thermal oxide film changes depending on the conditions such as the concentration of germanium in silicon-germanium, the substrate temperature, the temperature of pure water serving as a steam source, the flow rate of bubbling gas and oxidation time period. In the case where the thermal oxide film is used as the gate insulating film of the thin film transistor, a preferred thickness of the thermal oxide film is in the range of 50 nm to 200 nm. As a method for

thermally oxidizing the surface of the semiconductor layer **2**, pyrogenic oxidation or dry oxidation may be used instead of steam oxidation. However, an oxidation method using the steam obtained by bubbling is suitable for obtaining a thermal oxide film having good quality at a relatively low temperature, for example, at about 600°C or lower.

[0025] When silicon-germanium is thermally oxidized at about 700°C or higher, silicon is selectively oxidized rather than germanium. As a result, germanium is precipitated at the interface of semiconductor/insulating film or part containing a large amount of silicon and part containing a large amount of germanium are formed in a layered manner in the oxide film. Therefore, it is necessary to determine an oxidation temperature with care. The oxidation temperature is preferably 700°C or lower, more preferably, 600°C or lower.

[0026] Next, after a chromium (Cr) film having a thickness of about 200 nm is deposited onto the gate insulating film **3** by, for example, sputtering, the Cr film is patterned by photolithography and etching, thereby forming a gate electrode **4** as shown in Figure **1C**. Next, by using the gate electrode **4** as an implantation mask, impurity ions **5** acting as donors or acceptors are implanted into the semiconductor layer **2**. The impurity implantation is conducted by ion doping in which mass separation is not performed (alternatively, by bucket type ion doping method described in, for example, Extended Abstracts of the 22nd (1990) International Conference on Solid State Devices and Materials, p. 971 or p.1197). Plasma doping may be used instead of ion doping. Thereafter, a heat treatment (annealing) is conducted at a temperature in the range of about 300°C to 600°C so as to activate the impurities implanted into the semiconductor layer **2**, thereby forming a source region **6** and a drain region **6** as shown in Figure **1C**.

[0027] Next, after forming an interlevel insulating film **8** which consists of an SiO_2 film by an Atmospheric-Pressure CVD method, contact holes are formed in the interlevel insulating film **8**. Thereafter, a conductive film such as an aluminum (Al) film is formed on the interlevel insulating film **8** by sputtering. The conductive film is patterned by photolithography and etching so as to form a source electrode **9** and a drain electrode **10**, thereby forming a thin film transistor as shown in Figure **1D**.

[0028] In the thin film transistor of the present invention, the semiconductor layer **2** is made of silicon-germanium alloy, and the gate insulating film **3** is made of the thermal oxide film obtained by thermally oxidizing the surface of the semiconductor layer **2**. With this process, a cleaned interface of semiconductor/insulating film is formed. Therefore, a thin film transistor having excellent performance and high reliability can be fabricated. Furthermore, since the thin film transistor can be fabricated at a relatively low temperature, i.e., 600°C or lower, not only a low-cost glass substrate can be used, but also the production yield can be enhanced.

[0029] If dangling bonds, which are present at the grain boundaries of a polycrystalline film, are terminated by hydrogen, transistor characteristics are further improved. Therefore, it is desirable to perform a hydrogenation process. The hydrogenation process is carried out by exposing the substrate to hydrogen plasma or hydrogen atoms at a substrate temperature of about 300°C, at any stage from the formation step of the source region **6** and the drain region **7** to the completion of the thin film transistor.

[0030] Moreover, although the silicon-germanium film having a germanium concentration of 25% is used as the semiconductor layer **2** in Example 1, the semiconductor layer of the present invention is not limited to the concentration. Generally, in the case where the oxidation temperature is about 600°C, the oxidation rate is increased as the germanium concentration increases. As a result, the oxidation time period is shortened. Therefore, it is preferable that the semiconductor layer **2** is made of Si_xGe_{1-x} ($0 < x < 0.8$). Furthermore, since a field-effect mobility is increased as the germanium concentration increases, it is desirable that the germanium concentration is high. According to the present invention, a thin film transistor having the electron mobility of 50 $cm^2/V \cdot sec$ or more and the hole mobility of 30 $cm^2/V \cdot sec$ or more can be obtained.

[0031] In Example 1, a polycrystalline silicon-germanium layer, which is subjected to a crystallization process using a laser light, is used as the semiconductor layer **2**. A single-crystalline silicon-germanium layer, which is epitaxially grown on a single-crystalline semiconductor substrate, or a single-crystalline silicon-germanium layer having an SOI (Semiconductor On Insulator) structure may also be used.

[0032] Although Cr is used as a material of the gate electrode **4** and Al is used as a material of the source electrode **9** and the drain electrode **10** in Example 1, metals such as aluminum (Al), tantalum (Ta), molybdenum (Mo), chromium (Cr) and titanium (Ti), and alloys thereof may be used as electrode materials. Alternatively, heavily doped polycrystalline silicon, a polycrystalline silicon-germanium alloy, or transparent conductive layers such as ITO may also be used.

[0033] Furthermore, it is possible to adopt an LDD (lightly doped drain) structure in order to improve OFF characteristics of a transistor. It is also possible to selectively form a P-channel type transistor and an N-channel type transistor by selectively using, as impurities, boron, arsenic and the like acting as acceptors and phosphorous, aluminum and the like acting as donors. As a result, a CMOS circuit is integrated on the substrate.

Example 2

[0034] With reference to Figure **2A**, a second example of a thin film semiconductor device according to the present invention will be described.

[0035] In this example, a glass substrate (for exam-

ple, glass #1733, fabricated by Corning Inc.) **1**, on which an SiO_2 film acting as a buffer layer (not shown) is deposited in order to prevent the diffusion of impurities from the glass substrate, is used.

[0036] First, an amorphous silicon-germanium film containing germanium at a concentration of 50% (hereinafter, referred to as an "a-$Si_{0.50}Ge_{0.50}$" film) is formed on the glass substrate **1** to a thickness of 100 nm. The a-$Si_{0.50}Ge_{0.50}$ film is formed by CVD method using, for example, disilane (Si_2H_6) and germane (GeH_4) as material gases. Typically, the flow rate of disilane is in the range of 20 to 50 sccm, and the flow rate of germane is 20 to 50 sccm. It goes without saying that the flow rate of the gas changes depending on the size of the chamber and the like. It is preferable that the temperature of the glass substrate **1** during growth of the film is set to be in the range of 450°C to 600°C.

[0037] Next, the a-$Si_{0.50}Ge_{0.50}$ film is patterned to form an island region having the size in accordance with the size of a transistor to be formed. In Figure **2A**, only one island region is shown. In actual, however, a plurality of island regions may be simultaneously formed. The a-$Si_{0.50}Ge_{0.50}$ film can be carried out using the same photolithography and etching as those of Example 1.

[0038] Next, a heat treatment is conducted at, for example, 550°C, thereby obtaining a semiconductor layer **2a** made of polycrystalline silicon-germanium (hereinafter, referred to as "poly-$Si_{0.50}Ge_{0.50}$"). This heat treatment can be conducted by using a conventional electric furnace in a vacuum atmosphere or an inert gas atmosphere.

[0039] Next, the glass substrate 1 is inserted into a furnace at 550°C. Pure water held at 95°C is subjected to bubbling with nitrogen or gaseous oxygen. By using steam obtained by the bubbling, the surface of the semiconductor layer **2a** is thermally oxidized for two hours in the furnace. By the thermal oxidation, a thermal oxide film having a thickness of about 100 nm is formed. The thus obtained thermal oxide film, which is made of $Si_{0.50}Ge_{0.50}O_2$, is used as a gate insulating film 3.

[0040] Subsequently, a gate electrode **4**, a source region **6a**, a drain region **7a**, an insulating film **8**, a source electrode **9** and a drain electrode **10** are formed in the same manner as that of Example 1, thereby obtaining a thin film transistor shown in Figure **2A**.

[0041] Although the polycrystalline silicon-germanium layer, which is crystallized by heat treatment, is used as the semiconductor layer **2a**, a single-crystalline silicon-germanium layer may also be used. Moreover, the polycrystalline silicon-germanium layer, which is crystallized by laser irradiation, may also be used.

[0042] The gate insulating film **3** is formed by thermally oxidizing the semiconductor layer **2** containing germanium at a concentration of 25% at 600°C for two hours in Example 1, and is formed by thermally oxidizing the semiconductor layer **2a** containing germanium at a concentration of 50% at 550°C for two hours in Example 2. The oxidation temperature of Example 2 is lower than that of Example 1. When the oxidation temperature is low, the oxidation rate also decreases. However, the decrease in the oxidation rate is compensated by enhancing the germanium concentration, thereby holding the same oxidation time period.

Example 3

[0043] With reference to Figure **2B**, a third example of a thin film semiconductor device according to the present invention will be described.

[0044] In this example, a glass substrate (for example, glass #1733, fabricated by Corning Inc.) **1**, on which an SiO_2 film acting as a buffer layer (not shown) is deposited in order to prevent the diffusion of an impurity from the glass substrate, is used.

[0045] The thin film transistor of Example 3 differs from those described in the preceding examples in that the thin film transistor of Example 3 has a gate insulating film having a double-layered structure. More specifically, a second gate insulating film **11** which consists of a silicon nitride (SiN_x) layer is formed on a first gate insulating film **3a** ($Si_{0.50}Ge_{0.50}O_2$) serving as a thermal oxide film.

[0046] First, an amorphous silicon-germanium film containing germanium at a concentration of 50% (hereinafter, referred to as an "a-$Si_{0.50}Ge_{0.50}$" film) is formed on the glass substrate **1** to a thickness of 100 nm. The a-$Si_{0.50}Ge_{0.50}$ film is formed by a CVD method using, for example, disilane (Si_2H_6) and germane (GeH_4) as material gases. Typically, the flow rate of disilane is in the range of 20 to 50 sccm, and the flow rate of germane is 20 to 50 sccm. It goes without saying that the flow rate of the gas changes depending on the size of the chamber and the like. It is preferable that the temperature of the glass substrate **1** during growth of the film is set to be in the range of 450°C to 600°C.

[0047] Next, the a-$Si_{0.50}Ge_{0.50}$ film is patterned to form an island region having the size in accordance with the size of a transistor element to be formed. In Figure **2B**, only one island region is shown. In actual, however, a plurality of island regions may be simultaneously formed. The a-$Si_{0.50}Ge_{0.50}$ thin film can be carried out using the same photolithography and etching as those of the preceding examples.

[0048] Next, a heat treatment is conducted at, for example, 550°C, thereby obtaining a semiconductor layer **2** made of polycrystalline silicon-germanium (hereinafter, referred to as "poly-$Si_{0.50}Ge_{0.50}$").

[0049] Then, the glass substrate **1** is inserted into a furnace at 550°C. Pure water held at 95°C is subjected to bubbling with nitrogen or gaseous oxygen. By using steam obtained by the bubbling, the surface of the semiconductor layer **2** is thermally oxidized for two hours in the furnace. By the thermal oxidation, a thermal oxide film having a thickness of about 100 nm is formed. The thus obtained thermal oxide film, which is made of $Si_{0.50}Ge_{0.50}O_2$, is used as a first gate insulating film **3a**.

The thickness of the thermal oxide film changes depending on the conditions such as the concentration of germanium in silicon-germanium, the substrate temperature, the temperature of pure water serving as a steam source, the flow rate of bubbling gas, and oxidation time period. Next, a silicon nitride (SiN_x) layer is formed to a thickness of 100 nm by a CVD method, thereby obtaining the second insulating film **11**. After the step of forming the gate electrode **4**, the same steps as those of Examples 1 and 2 are carried out, thereby forming the thin film transistor shown in Figure **2B**.

[0050] The following advantageous effects can be obtained owing to the double-layered structure of the gate insulating film.

[0051] The insulation properties of the gate insulating films are improved, and therefore, the production yield is further improved. Moreover, owing to the second gate insulating film **11**, the thermal oxide film (first gate insulating film) can be thinned. Thus, a time period required for thermal oxidation can be reduced. Although the oxidation is performed at 550°C for two hours in Example 3, the thermal oxidation time may be shortened to about an hour. If the oxidation time is shortened, the processing throughput is improved.

[0052] Although a silicon nitride film is used as the second gate insulating film **11** in Example 3, other insulating films such as an SiO_2 film, a TaO_x film may also be used.

[0053] Although solid-phase growth by heat treatment is used as a method for obtaining a polycrystalline silicon-germanium layer as the semiconductor layer **2a**, the semiconductor layer **2a** can also be obtained by crystallization with laser irradiation. Moreover, a single-crystalline silicon--germanium layer may also be used as the semiconductor layer **2a**.

[0054] Regarding the ratio of silicon and germanium which serve as the semiconductor layer **2** or **2a**, the germanium concentration is preferably 20% or higher in terms of mobility. The reason for this is that carriers (electrons or holes) are scattered at the germanium concentration of 20% or lower, resulting in the lowered mobility. On the other hand, in terms of oxidation, it is desirable that the germanium concentration is high.

[0055] In the case where the semiconductor layer **2** or **2a** is formed by laser irradiation, although the crystallization can be advantageously performed at room temperature, the crystal grain size cannot be formed so large. On the other hand, in the case where the semiconductor layer **2** or **2a** is formed by heat treatment, although a relatively high temperature (about 550°C) is required, the crystal grain has a large size, i.e., about one to several tens μm. As the crystal grain size becomes large, the mobility is further improved.

[0056] Although the glass substrate is used in the above examples, any substrate can be used as long as it has an insulating surface. For example, a normal single-crystalline silicon substrate, whose upper surface is covered with an insulating film, may also be used. In such a case, a device, in which a transistor formed on the single-crystalline silicon substrate and the thin film semiconductor device according to the present invention are integrated on the same substrate, is provided.

[0057] In the above examples, the case where the Si_xGe_{1-x} layer is used as an active layer of the thin film transistor and the $Si_xGe_{1-x}O_2$ thermal oxide film is used as a gate insulating film is described. However, it is also possible to use the Si_xGe_{1-x} layer as a conductive part of the gate electrode or the wiring in the semiconductor device, and the $Si_xGe_{1-x}O_2$ thermal oxide film as an insulating covering part of the conductive part. In such a case, appropriate impurities are doped into the semiconductor layer.

Example 4

[0058] With reference to Figures **3A** to **3D**, a fourth example of a thin film semiconductor device according to the present invention will be described.

[0059] A field oxide film **33** with an n^+-channel stopper **34** is formed on an n^--type silicon substrate **32** by a LOCOS (Local Oxidation Of Silicon) method so as to surround an active region on which an MOS transistor is to be formed. Next, a gate oxide film **35** is formed by thermal oxidation to a thickness of 10 to 30 nm. A polycrystalline silicon-germanium film is deposited to a thickness of 300 nm by using, for example, silane (SiH_4) and germane (GeH_4) as material gases. Typically, the flow rate of disilane is in the range of 20 to 50 sccm, and the flow rate of germane is 20 to 50 sccm. It goes without saying that the flow rate of the gas changes depending on the size of the chamber and the like. It is preferable that the temperature of the silicon substrate **32** during growth of the film is set to be in the range of 600°C to 650°C.

[0060] Next, exposed portions of the gate oxide film **35** are selectively removed by etching using a gate electrode as a mask. After depositing an SiO_2 film on the substrate **32** by a CVD method, sidewall spacers **37** are formed by etching back the SiO_2 film (Figure **3A**). Next, for example, boron (B) ions **38** are implanted into the substrate **32** to form a p^+-region (source/drain region) **39** by using the gate electrode and the spacer as masks (Figure **3B**). The dose of ions is reduced below the spacers **37** to form p^--regions **40**. As a result, an LDD (Lightly Doped Drain) structure is formed for alleviating electric field at the end of the drain region.

[0061] Then, the silicon substrate **32** is inserted into a furnace at 600°C. Pure water held at 95°C is subjected to bubbling with nitrogen or gaseous oxygen. By using steam obtained by the bubbling, the surface of the polycrystalline silicon-germanium film layer is thermally oxidized for two hours in the furnace. By the thermal oxidation, a silicon-germanium oxide film **41** is formed (Figure **3C**). Silicon is hardly oxidized at the oxidation temperature. Only the polycrystalline silicon-germanium serving as the gate electrode is selectively oxidized. As a result, the gate electrode is electrically isolated without

forming the interlevel insulating layer. Moreover, since the oxidation is conducted at 600°C, lateral diffusion of implanted boron ions is restrained to reduce parasitic capacitance and the like. As a result, device characteristics are improved. After forming a through hole **42**, metallization is conducted with aluminum so as to form a source electrode **43**, a drain electrode **44** and a gate electrode **45**, thereby completing a p-type MOS transistor (Figure **3D**).

[0062] Although the through hole **42** is formed and the metallization for forming source/drain regions is conducted immediately after the polycrystalline silicon-germanium film is oxidized, the following process is also applicable. After the polycrystalline silicon-germanium film is oxidized, an insulating layer made of SiO_2 and Si_3N_4 is deposited by a CVD method. Thereafter, a through hole is formed. In this way, the production yield is further improved.

[0063] The method for forming the p-channel MOS transistor alone is described in Example 4. However, an n-channel MOS transistor or a CMOS structure can be produced by the same method. Furthermore, the method is also applicable to semiconductor devices other than the MOS transistor.

[0064] According to the present invention, a layer containing silicon and germanium is used as a semiconductor layer, and a thermal oxide film, which is obtained by thermally oxidizing the surface of the semiconductor layer, serves as a gate insulating film. As a result, a cleaned interface of semiconductor/insulating film can be formed by a process at a relatively low temperature (600°C or lower). Therefore, a thin film semiconductor device can be fabricated with good production yield by using a relatively inexpensive glass substrate having a low strain point. Moreover, since the interface of semiconductor/insulating film can be held in a clean condition, it is possible to realize a thin film semiconductor device excellent in performance and reliability.

[0065] In the case where the layer containing silicon and germanium is used as a gate electrode or a wiring, since the surface of the electrode or the wiring is covered with a thermal oxide film of high quality, the electrode or the wiring, which is hardly short-circuited, can be obtained.

[0066] Various other modifications will be apparent to and can be readily made by those skilled in the art without departing from the scope of this invention. Accordingly, it is not intended that the invention be limited to the description as set forth herein, but rather should be limited only by the scope of the appended claims.

Claims

1. A thin film semiconductor device comprising:

   a substrate (1) having an insulating surface;
   a semiconductor layer (2, 2a) comprising Si_xGe_{1-x} formed on the substrate;
   a gate insulating film (3, 3a) formed on the semiconductor layer; and
   a gate electrode (4) formed on the gate insulating film, **characterised in that**
   the gate insulating film (3, 3a) includes a thermal oxide film comprising $Si_xGe_{1-x}O_2$, with $0 < x < 0.8$, formed by thermally oxidising a surface of the semiconductor layer (2, 2a); and the semiconductor layer comprising Si_xGe_{1-x}, with $0 < x < 0.8$.

2. A thin film semiconductor device according to claim 1, wherein the gate insulating film (3a) includes another insulating film (11) deposited on the thermal oxide film.

3. A thin film semiconductor device according to claim 2, the another insulating film (11) is made of silicon nitride, tantalum oxide or silicon dioxide.

4. A method of fabricating a semiconductor device, comprising the steps of:

   forming a semiconductor layer (2, 2a) comprising Si_xGe_{1-x}, with $0 < x < 0.8$, on a substrate (1) having an insulating surface;
   forming a thermal oxide film on a surface of the semiconductor layer, the thermal oxide film comprising $Si_xGe_{1-x}O_2$, with $0 < x < 0.8$;
   forming a gate electrode (4) on the thermal oxide film; and
   forming a source region (6, 6a) and a drain region (7, 7a) in the semiconductor layer (2, 2a) by doping impurities acting as donors or acceptors in selected regions of the semiconductor layer.

5. A method of fabricating a semiconductor device according to claim 4, wherein the semiconductor layer (2, 2a) is annealed with an energy beam after formation of the semiconductor layer and prior to formation of the thermal oxide film, thereby melting/solidifying the semiconductor layer.

6. A method of fabricating a semiconductor device according to claim 4, wherein the semiconductor layer (2, 2a) is formed in an amorphous state, and the semiconductor layer is annealed after formation of the semiconductor layer and prior to formation of the thermal oxide film, thereby rendering the semiconductor layer polycrystalline or single-crystalline.

7. A method of fabricating a semiconductor device according to claim 4, wherein the thermal oxide film is grown at 700° C or lower.

8. A method of fabricating a semiconductor device ac-

cording to claim 5, wherein the thermal oxide film is grown at 700° C or lower.

9. A method of fabricating a semiconductor device according to claim 6, wherein the thermal oxide film is grown at 700° C or lower.

Patentansprüche

1. Dünnfilm-Halbleiteranordnung mit

einem Substrat (1) mit einer isolierenden Oberfläche;
einer Halbleiter-Schicht (2, 2a) mit Si_xGe_{1-x}, die auf dem Substrat ausgebildet ist;
einem Tor- bzw. Gate- isolierenden Film (3, 3a), der auf der Halbleiter-Schicht ausgebildet ist; und
einer Gate- bzw. Steuer-Elektrode (4), die auf dem Gate- isolierenden Film ausgebildet ist, **dadurch gekennzeichnet**, dass
der Gate- isolierende Film (3, 3a) einen thermischen Oxid-Film mit $Si_xGe_{1-x}O_2$ mit $0< x < 0,8$ enthält, der durch thermisches Oxidieren einer Oberfläche der Halbleiter-Schicht (2, 2a) ausgebildet ist; und
dass die Halbleiter-Schicht Si_xGe_{1-x} mit $o <x < 0,8$ aufweist.

2. Dünnfilm-Halbleiteranordnung nach Anspruch 1, wobei der Gate- isolierende Film (3a) einen weiteren isolierenden Film (11) enthält, der auf dem thermischen Oxid-Film abgelagert ist.

3. Dünnfilm-Halbleiteranordnung nach Anspruch 2, wobei der weitere isolierende Film (11) aus Siliziumnitrid, Tantaloxid oder Siliziumdioxid hergestellt ist.

4. Verfahren zur Herstellung einer Halbleiteranordnung mit den Schritten:

Ausbilden einer Halbleiter-Schicht (2, 2a) mit Si_xGe_{1-x} mit $0 < x < 0,8$ auf einem Substrat (1) mit einer isolierenden Oberfläche;
Ausbilden eines thermischen Oxid-Film auf einer Oberfläche der Halbleiter-Schicht, wobei der thermische Oxid-Film $Si_xGe_{1-x}O_2$ mit $0 < x < 0,8$ aufweist;
Ausbilden einer Tor- bzw. Gate-Elektrode (4) auf dem thermischen Oxid-Film; und
Ausbilden eines Quellen- bzw. Source-Bereichs (6, 6a) und eines Drain-Bereichs (7, 7a) in der Halbleiter-Schicht (2, 2a) durch Dotieren von Verunreinigungen, die in ausgewählten Bereichen der Halbleiter-Schicht als Donatoren oder Akzeptoren wirken.

5. Verfahren zur Herstellung einer Halbleiteranordnung nach Anspruch 4, wobei die Halbleiter-Schicht (2, 2a) nach der Ausbildung der Halbleiter-Schicht und vor der Ausbildung des thermischen Oxid-Films mit einem Energie-Strahl wärmebehandelt bzw. geglüht wird, wodurch die Halbleiter-Schicht geschmolzen/erstarrt wird.

6. Verfahren zur Herstellung einer Halbleiteranordnung nach Anspruch 4, wobei die Halbleiter-Schicht (2, 2a) in einem amorphen Zustand ausgebildet wird, und wobei die Halbleiter-Schicht nach der Ausbildung der Halbleiter-Schicht und vor der Ausbildung des thermischen Oxid-Films geglüht bzw. wärmebehandelt wird, wodurch die Halbleiter-Schicht polykristallin oder einkristallin wird.

7. Verfahren zur Herstellung einer Halbleiteranordnung nach Anspruch 4, wobei der thermische Oxid-Film bei 700°C oder weniger aufgezogen wird.

8. Verfahren zur Herstellung einer Halbleiteranordnung nach Anspruch 5, wobei der thermische Oxid-Film bei 700°C oder weniger aufgezogen wird.

9. Verfahren zur Herstellung einer Halbleiteranordnung nach Anspruch 6, wobei der thermische Oxid-Film bei 700°C oder weniger aufgezogen wird.

Revendications

1. Dispositif à semiconducteur à couche mince comprenant :

un substrat (1) comportant une surface isolante,
une couche de semiconducteur (2, 2a) comprenant du Si_xGe_{1-x} formée sur le substrat,
un film isolant de grille (3, 3a) formé sur la couche de semiconducteur, et
une électrode de grille (4) formée sur le film isolant de grille, **caractérisé en ce que**
le film isolant de grille (3, 3a) comprend un film d'oxyde thermique comprenant $Si_xGe_{1-x}O_2$, avec $0 < x < 0,8$, formé en oxydant thermiquement une surface de la couche de semiconducteur (2, 2a), et la couche de semiconducteur comprenant Si_xGe_{1-x}, avec $0 < x < 0,8$.

2. Dispositif à semiconducteur à couche mince selon la revendication 1, dans lequel le film isolant de grille (3a) comprend un autre film isolant (11) déposé sur le film d'oxyde thermique.

3. Dispositif à semiconducteur à couche mince selon la revendication 2, l'autre film isolant (11) étant fait de nitrure de silicium, d'oxyde de tantale ou de

dioxyde de silicium.

4. Procédé de fabrication d'un dispositif à semiconducteur, comprenant les étapes consistant à :

former une couche de semiconducteur (2, 2a) comprenant Si_xGe_{1-x}, avec $0 < x < 0,8$, sur un substrat (1) comportant une surface isolante,
former un film d'oxyde thermique sur une surface de la couche de semiconducteur, le film d'oxyde thermique comprenant $Si_xGe_{1-x}O_2$, avec $0 < x < 0,8$,
former une électrode de grille (4) sur le film d'oxyde thermique, et
former une région de source (6, 6a) et une région de drain (7, 7a) dans la couche de semiconducteur (2, 2a) en dopant par des impuretés agissant comme donneurs ou accepteurs dans des régions sélectionnées de la couche de semiconducteur.

5. Procédé de fabrication d'un dispositif à semiconducteur selon la revendication 4, dans lequel la couche de semiconducteur (2, 2a) est recuite avec un faisceau énergétique après formation de la couche de semiconducteur et avant la formation du film d'oxyde thermique, en fondant/solidifiant ainsi la couche de semiconducteur.

6. Procédé de fabrication d'un dispositif à semiconducteur selon la revendication 4, dans lequel la couche de semiconducteur (2, 2a) est formée dans un état amorphe, et la couche de semiconducteur est recuite après formation de la couche de semiconducteur et avant la formation du film d'oxyde thermique, en rendant ainsi la couche de semiconducteur polycristalline ou monocristalline.

7. Procédé de fabrication d'un dispositif à semiconducteur selon la revendication 4, dans lequel le film d'oxyde thermique est mis en croissance à 700 °C ou moins.

8. Procédé de fabrication d'un dispositif à semiconducteur selon la revendication 5, dans lequel le film d'oxyde thermique est mis en croissance à 700 °C ou moins.

9. Procédé de fabrication d'un dispositif à semiconducteur selon la revendication 6, dans lequel le film d'oxyde thermique est mis en croissance à 700 °C ou moins.

FIG.1A

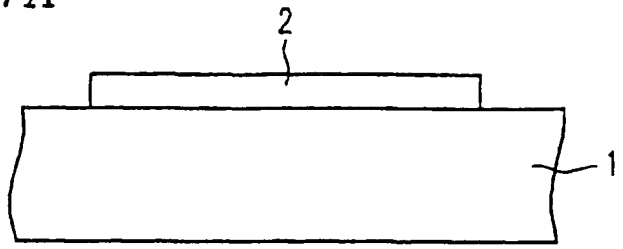

FIG.1B

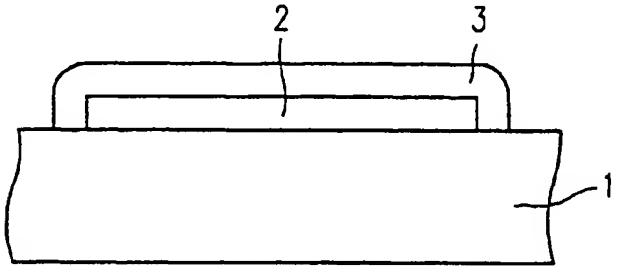

FIG.1C

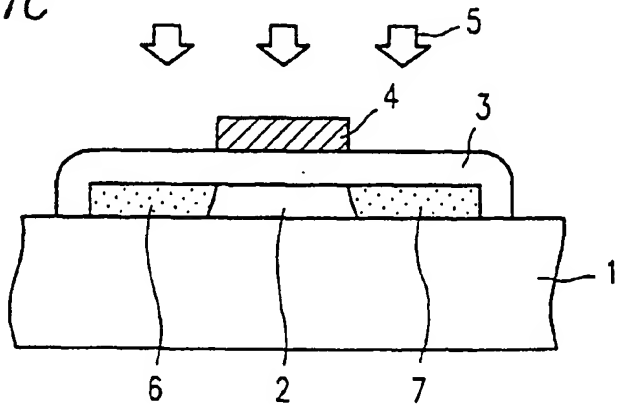

FIG.1D

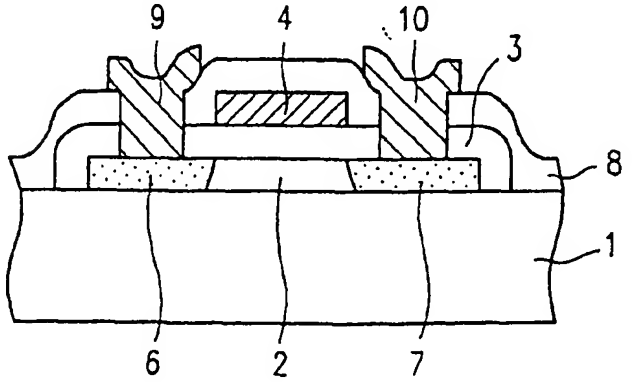

FIG. 2A

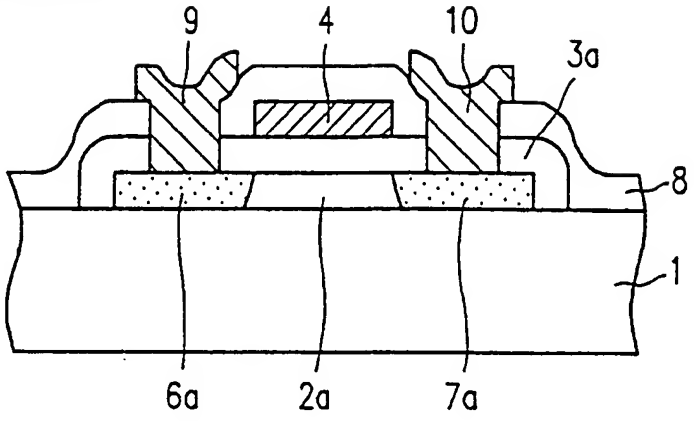

FIG. 2B

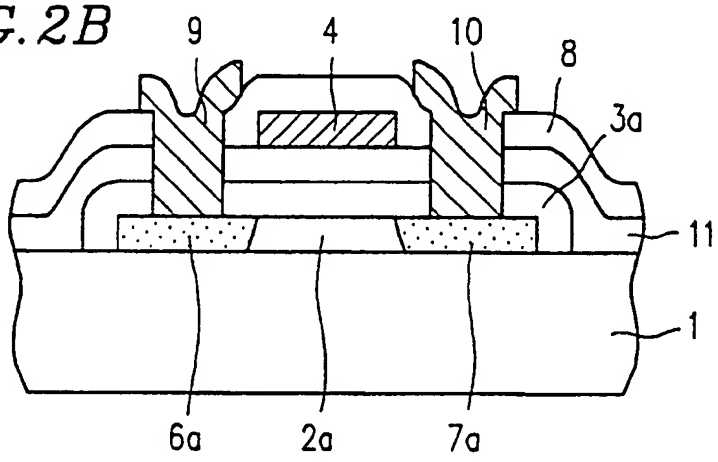

FIG. 3A

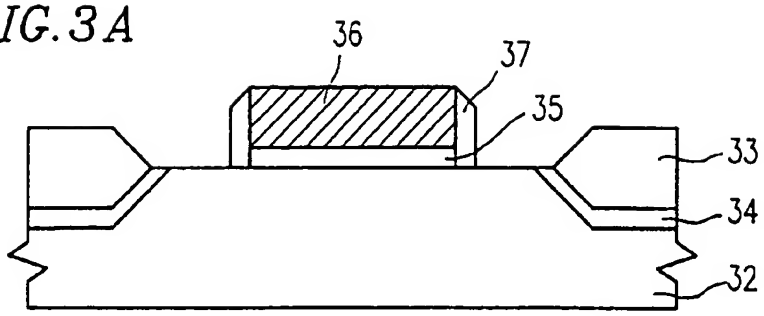

FIG. 3B

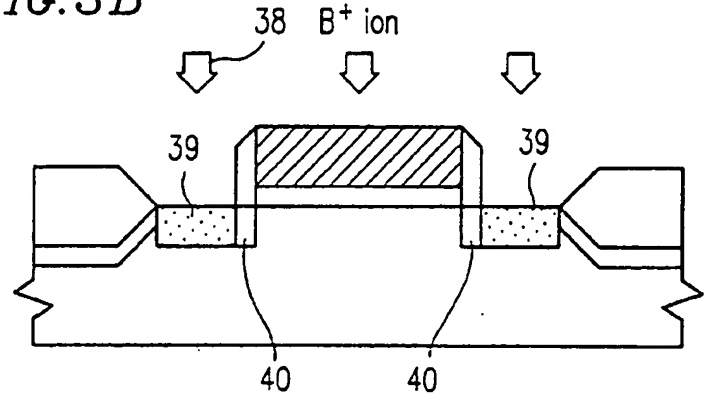

FIG. 3C

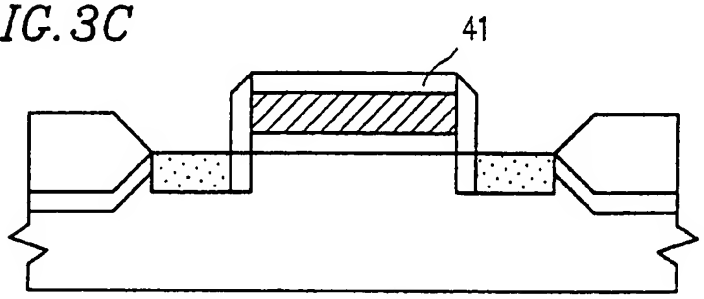

FIG. 3D

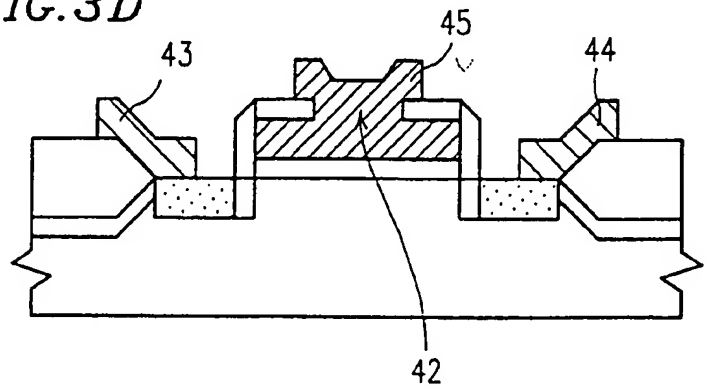

FIG. 4A

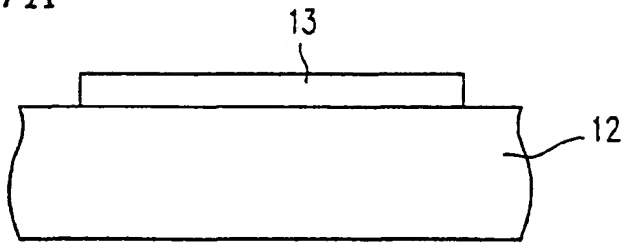

FIG. 4B

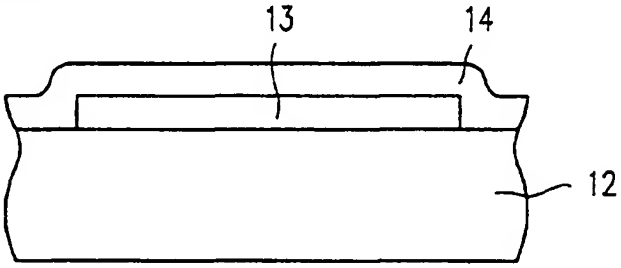

FIG. 4C

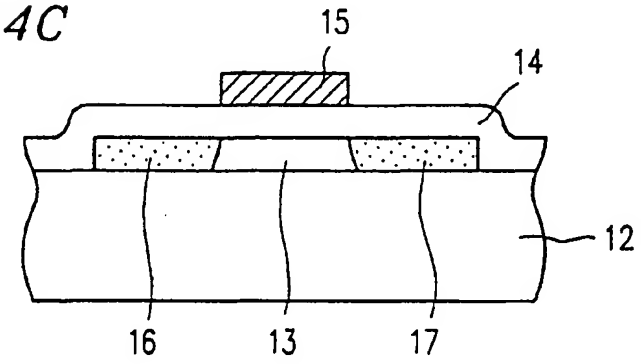

FIG. 4D